REMARKS

Applicants again thank Examiner for the careful examination of this application and the clear explanation of the rejections.

As amended, claim 1 describes a method for forming shallow trench isolation structures. The method forms a plurality of isolation trenches in a substrate in order to separate the active areas. The method then forms an insulation layer outwardly from the substrate. The insulation layer, which conforms to the contour of the outward surface of the substrate, fills the isolation trenches and covers the active areas. The method then forms a planarization layer outwardly from the insulation layer.

The choice of material and the method of applying the planarization layer is such that upon forming, its outward surface is substantially flat. The method then removes the planarization layer and the insulation layer, by a removing process that removes the planarization layer and the insulation layer at substantially the same rate.

In contrast, the Lin reference teaches a shallow trench isolation process using chemical mechanical polish and a nitride mask on HDP-oxide that is self-aligned. It accomplishes this by planarizing an oxide layer 40 to form shallow trench isolation between active areas 12 in a substrate. The method taught in the Lin reference uses a chemical mechanical polish (CMP) step to form openings 50 over "wide" active areas 12A. A key feature of the invention is the "non-conformal" oxide layer 40 that allows opening 50 to be formed only over wide active areas 12A,

and not over other active areas. As depicted in Fig. 1, a protrusion exists above the "wide" active area 12A but not above other active areas 12B. Therefore the layer 40 is non-conformal to the areas 12A but must be conformal to the wide active area 12A.

An etch barrier layer 44 is then deposited over the first insulating layer 40. Unlike the planarization layer in Applicants' invention, the etch barrier layer 44 must be conformal to the varying contour between 12A area and 12B area.

The Lin reference next uses a CMP to chemical-mechanical polish the raised portions of the conformal etch barrier layer to form a first opening 50 to expose the first insulating layer 40 over the wide active area 12A. The method uses this self-aligned opening 50 for etching the first insulating layer 40.

The key feature in the Lin reference is that the surface of the etch barrier layer 44, which is conformal and which Examiner equates to our planarization layer, must conform to the contour of the insulating layer 40 and faithfully reflect the raised contour at 12A over the "wide" active areas, as depicted in Figure 2 in the Lin reference. In contrast, in our invention, the outward surface of the planarization layer is substantially flat, as illustrated in the embodiment depicted in Figure 1C. Lin's method cannot function with Applicants' invention. Therefore, the Lin reference does not anticipate Applicants' invention and claim 1 stands patentable.

Claims 2-11 are dependent claims based on claim 1 and further include additional limitation not taught in the

reference. Particularly, claim 2 claims the method in which the removing the planarization layer and the insulation layer further comprises etching through the planarization layer and the insulation layer down to a chemical mechanical polishing (CMP) depth outward from the active areas and then chemical mechanically polishing it down to the polish stop layer. Claims 3 and 5 further limit the relative etch rates in the method. Claim 4 further limits the matched etch to comprise a resist etch back plasma etch. Claim 6 further includes the removal of the polish stop layer. Claim 8 further limits the polish stop to comprise silicon nitride. Claim 9 further limits the insulation layer to comprise silicon oxide. Claim 11 further limits the CMP depth to be between 1,000 and 1,500 angstroms. Claims 2 through 12 are not anticipated nor suggested by the Lin reference and stand patentable over the Lin reference.

Claim 13 describes a method for forming an integrated circuit. The method forms a plurality of isolation trenches in a substrate in order to separate the active areas. The method then forms an insulation layer outwardly from the substrate. The insulation layer fills the isolation trenches and covers the active areas and it substantially conforms to the contour of the substrate surface. The method then forms outwardly from the insulation layer a planarization layer of which the outward surface is substantially flat. The method then etches through the planarization layer and the insulation layer down to a chemical mechanical polishing (CMP) depth from the active areas. The etching process etches the planarization layer and the insulation layer at

substantially the same rate. The method then chemically-mechanically polishes from the CMP depth down to a polish stop above the active areas. The method then forms integrated circuit devices in the active areas to form an integrated circuit on the substrate.

Claim 13 includes the limitation of forming a planarization layer outwardly from the insulation layer and the layer having an outward surface that is substantially flat. Claim 13 also includes the limitation of etching through the planarization layer and the insulation layer by an etching process that etches the two layers at substantially the same rate.

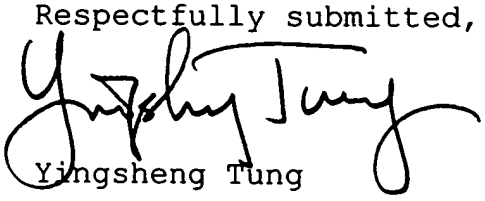
The Lin reference does not include those limitations and the Lin method cannot operate with Applicants' invention for the same reason stated above. Therefore, the Lin reference does not anticipate claim 13 and it stands patentable.

Claims 14-20 depend on claim 13 and include further limitations not taught in the Lin reference. Claims 14-20 stand patentable.

Applicants respectfully assert that the application is in allowable form and the claims distinguish over the cited

reference. Applicants respectfully request the reconsideration or further examination of this application.

Respectfully submitted,



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Version with Markings to show Changes made in the Claims

1. A method for forming shallow trench isolation structures, comprising:

forming a plurality of isolation trenches in a substrate, the isolation trenches separating active areas;

forming an insulation layer outwardly from the substrate, the insulation layer filling the isolation trenches and covering the active areas and substantially conforming to the substrate surface contour;

forming a planarization layer outwardly from the insulation layer, the planarization layer having an outward surface that is substantially flat; and

removing the planarization layer and the insulation layer by a removing process that removes the planarization layer and the insulation layer at substantially the same rate. [down to a polished stop for the active areas.]

2. The method of Claim 1, wherein removing the planarization layer and the insulation layer further comprises:

etching through the planarization layer and the insulation layer together [at a substantially even rate] down to a chemical mechanical polishing (CMP) depth outward from the active areas; and

chemically-mechanically polishing from the CMP depth down to the polish stop [for] layer above the active areas.

13. A method for forming an integrated circuit, comprising:

forming a plurality of isolation trenches in a substrate, the isolation trenches separating active areas;

forming an insulation layer outwardly from the substrate, the insulation layer filling the isolation trenches and covering the active areas and substantially conforming to the substrate surface contour;

forming a planarization layer outwardly from the insulation layer, the planarization layer having an outward surface that is substantially flat;

etching through the planarization layer and the insulation layer [together at a substantially even rate] by an etching process that etches the planarization layer and the insulation layer at substantially the same rate, down to a chemical mechanical polishing (CMP) depth outward from the active areas;

chemically-mechanically polishing from the CMP depth down to a polish stop for the active areas; and

forming integrated circuit devices in the active areas to form an integrated circuit on the substrate.

14. The method of Claim 13, further comprising etching through the planarization layer and the insulation layer [at the substantially even rate] using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by ten percent or less.

15. The method of Claim 13, further comprising etching through the planarization layer and the insulation layer [at the substantially even rate] using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by five percent or less.